What is claimed is:

1. An optoelectronic integrated circuit comprising:
a) a substrate;
b) a multilayer structure formed on said substrate; and
c) an array of thyristor devices and corresponding resonant cavities formed in said multilayer structure, said resonant cavities adapted to process different wavelengths of light.

2. An optoelectronic integrated circuit according to claim 1, wherein:
portions of said multilayer structure are removed to provide said resonant cavities with different vertical dimensions that correspond to said different wavelengths.

3. An optoelectronic integrated circuit according to claim 1, wherein:
said portions of said multilayer structure that are removed to provide said resonant cavities with different vertical dimensions comprise a periodic substructure formed by repeating pairs of an undoped spacer layer and an undoped etch stop layer.

4. An optoelectronic integrated circuit according to claim 3, wherein:
said multilayer structure comprises strained silicon materials.

5. An optoelectronic integrated circuit according to claim 3, wherein:
said multilayer structure comprises group III-V materials.

6. An optoelectronic integrated circuit according to claim 5, wherein
said undoped spacer layer comprises undoped GaAs, and said undoped etch stop layer comprises undoped AlAs that functions as an etch stop during etching by a chlorine-based gas mixture that includes fluorine.

7. An optoelectronic integrated circuit according to claim 1, wherein:

each given thyristor device of said array is configured as a vertical cavity lasing device to thereby provide an array of vertical cavity lasing devices that emit light at different wavelengths.

8. An optoelectronic integrated circuit according to claim 1, wherein:

each given thyristor device of said array is configured as an optical detecting device to thereby provide an array of optical detectors that detect input optical pulses at different wavelengths and produces corresponding output pulses.

9. An optoelectronic integrated circuit according to claim 8, wherein:

said output pulses are electrical output pulses that correspond to detected input optical pulses at different wavelengths.

10. An optoelectronic integrated circuit according to claim 8, wherein:

said output pulses are optical output pulses that correspond to detected input optical pulses at different wavelengths.

11. An optoelectronic integrated circuit according to claim 1, wherein:

each given thyristor device of said array comprises a n-type modulation doped quantum well structure and a p-type modulation doped quantum well structure.

12. An optoelectronic integrated circuit according to claim 11, further comprising:

a current source operably coupled to at least one of said n-type modulation doped quantum well structure and a p-type modulation doped quantum well structure.

13. An optoelectronic integrated circuit according to claim 12, wherein:

each given thyristor device comprises a p-channel FET transistor formed on said substrate and an n-channel FET transistor formed atop said p-channel FET transistor, said p-channel FET transistor formed from said p-type modulation doped quantum well structure and said n-channel FET transistor formed from said n-type modulation doped quantum well structure.

14. An optoelectronic integrated circuit according to claim 13, wherein:

said p-channel FET transistor includes a bottom active layer,

said n-channel FET transistor includes a top active layer, and

said given thyristor device further comprises an anode terminal operably coupled to said top active layer, a cathode terminal operably coupled to said bottom active layer, and an injector terminal operably coupled to at least one of said n-type modulation doped quantum well structure and said p-type doped p-type quantum well structure.

15. An optoelectronic integrated circuit according to claim 14, wherein:

said injector terminal is operably coupled to said n-type modulation doped quantum well structure via at least one n-type ion implant into said n-type modulation doped quantum well structure.

16. An optoelectronic integrated circuit according to claim 14, wherein:

said injector terminal is operably coupled to said p-type modulation doped quantum well structure via at least one p-type ion implant into said p-type modulation doped quantum well structure.

17. An optoelectronic integrated circuit according to claim 14, wherein:

said given thyristor device further comprises an ohmic contact layer, a metal layer for said anode terminal that is formed on said ohmic contact layer, and a plurality of p-type layers formed between said ohmic contact layer and said n-type modulation doped quantum well structure.

18. An optoelectronic integrated circuit according to claim 17, further comprising:

n-type implants disposed below said metal layer for said anode terminal to thereby provide for current funneling into an active area of said given thyristor device.

19. An optoelectronic integrated circuit according to claim 17, wherein:

said plurality of p-type layers are separated from said n-type modulation doped quantum well structure by undoped spacer material.

20. An optoelectronic integrated circuit according to claim 17, wherein:

said plurality of p-type layers include a top sheet and bottom sheet of planar doping of highly doped p-material separated by a lightly doped layer of p-material, whereby said top sheet achieves low gate contact resistance and said bottom sheet defines the capacitance of said n-channel FET transistor.

21. An optoelectronic integrated circuit according to claim 14, further comprising:

a current source operably coupled to said injector terminal that draws bias current from a quantum well structure coupled thereto, and

a load resistor operably coupled to said cathode terminal that biases said thyristor device such that a forward bias exists between said anode and cathode terminals that is less than maximum forward switching voltage of the thyristor device.

22. An optoelectronic integrated circuit according to claim 21, wherein:

said given thyristor device is configured as an optical detector that detects an incident optical pulse of sufficient intensity at an associated wavelength and produces a corresponding output electrical pulse at the cathode terminal of said given thyristor device.

23. An optoelectronic integrated circuit according to claim 21, wherein:

said given thyristor device is configured such that when said incident optical pulse has sufficient intensity at the associated wavelength, photocurrent is produced in said quantum well channel in excess of said bias current to produce a channel charge that exceeds a critical switching charge, thereby causing said thyristor device to switch to the ON state, and when the incident optical pulse is terminated, the bias current switches the thyristor device to the OFF state.

24. An optoelectronic integrated circuit according to claim 21, wherein:

said given thyristor device is configured as a laser emitter that emits an output optical pulse at an associated wavelength in response to an input electrical pulse supplied to the injector terminal.

25. An optoelectronic integrated circuit according to claim 21, wherein:

said given thyristor device is configured such that said input electrical pulse produces current in said quantum well channel in excess of said bias current to produce a channel charge that exceeds a critical switching charge, thereby causing said thyristor device to switch to the ON state, and when the input electrical pulse is terminated, the bias current switches the thyristor device to the OFF state, and wherein current through the given thyristor device in the ON state is greater than a characteristic lasing threshold current for the given thyristor device.

26. An optoelectronic integrated circuit according to claim 1, wherein:

said resonant cavities comprise a bottom distributed bragg reflector mirror and a top dielectric mirror.

27. An optoelectronic integrated circuit according to claim 26, wherein:

said thyristor devices are formed from an active device structured disposed between said bottom distributed bragg reflector mirror and said top dielectric mirror, and said portions of said multilayer structure that are removed to provide said resonant cavities with different vertical dimensions are disposed between said active device structure and said top dielectric mirror.

28. An optoelectronic integrated circuit according to claim 26, further comprising:

means for passing light through one of said top dielectric mirror and said bottom distributed bragg reflector mirror through which incident light is injected into said resonant cavity and/or through which light produced in said resonant cavity is emitted.

29. An optoelectronic integrated circuit according to claim 26, further comprising:

a plurality of diffraction gratings formed under said top dielectric mirror, wherein said diffraction gratings inject incident light that is propagating along an in-plane direction into the resonant cavities, and emits light produced in the resonant cavities along an in-plane direction.

30. A method of fabricating an optoelectronic integrated circuit comprising:

a) providing a substrate;

b) forming a multilayer structure on said substrate; and

c) forming an array of thyristor devices and corresponding resonant cavities in said multilayer structure, said resonant cavities adapted to process different wavelengths of light.

31. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

portions of said multilayer structure are selectively removed to provide said resonant cavities with different vertical dimensions that correspond to said different wavelengths.

32. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

said multilayer structure comprises a periodic substructure formed by repeating pairs of an undoped spacer layer and an undoped etch stop layer.

33. A method of fabricating an optoelectronic integrated circuit according to claim 32, further comprising:

selectively removing portions of said periodic substructure to provide said resonant cavities with different vertical dimensions that correspond to said different wavelengths.

34. A method of fabricating an optoelectronic integrated circuit according to claim 32, wherein:

said multilayer structure comprises strained silicon materials.

35. A method of fabricating an optoelectronic integrated circuit according to claim 32, wherein:

said multilayer structure comprises group III-V materials.

36. A method of fabricating an optoelectronic integrated circuit according to claim 35, wherein:

said undoped spacer layer comprises undoped GaAs, and said undoped etch stop layer comprises undoped AlAs that functions as an etch stop during etching by a chlorine-based gas mixture that includes fluorine.

37. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

each given thyristor device of said array is configured as a vertical cavity lasing device to thereby provide an array of vertical cavity lasing devices that emit light at different wavelengths.

38. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

each given thyristor device of said array is configured as an optical detecting device to thereby provide an array of optical detectors that detect input optical pulses at different wavelengths and produces corresponding output pulses.

39. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

said output pulses are electrical output pulses that correspond to detected input optical pulses at different wavelengths.

40. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

said output pulses are optical output pulses that correspond to detected input optical pulses at different wavelengths.

41. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

each given thyristor device of said array comprises a n-type modulation doped quantum well structure and a p-type modulation doped quantum well structure.

42. A method of fabricating an optoelectronic integrated circuit according to claim 41, further comprising:

coupling a current source to at least one of said n-type modulation doped quantum well structure and a p-type modulation doped quantum weii structure.

43. A method of fabricating an optoelectronic integrated circuit according to claim 41, wherein:

each given thyristor device comprises a p-channel FET transistor formed on said substrate and an n-channel FET transistor formed atop said p-channel FET transistor, said p-channel FET transistor formed from said p-type modulation doped quantum well structure and said n-channel FET transistor formed from said n-type modulation doped quantum well structure.

44. A method of fabricating an optoelectronic integrated circuit according to claim 43, wherein:

said p-channel FET transistor includes a bottom active layer,

said n-channel FET transistor includes a top active layer, and

said given thyristor device further comprises an anode terminal operably coupled to said top active layer, a cathode terminal operably coupled to said bottom active layer, and an injector terminal operably coupled to at least one of said n-type modulation doped quantum well structure and said p-type doped p-type quantum well structure.

45. A method of fabricating an optoelectronic integrated circuit according to claim 44, further comprising:

implanting n-type ions into said n-type modulation doped quantum well structure to form at least one n-type implant that couples said injector terminal to said n-type modulation doped quantum well structure.

46. A method of fabricating an optoelectronic integrated circuit according to claim 44, further comprising:

implanting p-type ions into said p-type modulation doped quantum well structure to form at least one p-type implant that couples said injector terminal to said p-type modulation doped quantum well structure.

47. A method of fabricating an optoelectronic integrated circuit according to claim 44, wherein:

said given thyristor device further comprises an ohmic contact layer, a metal layer for said anode terminal that is formed on said ohmic contact layer, and a plurality of p-type layers formed between said ohmic contact layer and said n-type modulation doped quantum well structure.

48. A method of fabricating an optoelectronic integrated circuit according to claim 47, further comprising:

implanting n-type ions into said multilayer structure to form n-type implants that are adjacent to an active area of said given thyristor device, and

depositing and patterning said metal layer for said anode terminal such that it is disposed over said n-type implants, such that said n-type implants provide for current funneling into said active area of said given thyristor device.

49. A method of fabricating an optoelectronic integrated circuit according to claim 47, wherein:

said plurality of p-type layers are separated from said n-type modulation doped quantum well structure by undoped spacer material.

50. A method of fabricating an optoelectronic integrated circuit according to claim 47, wherein:

said plurality of p-type layers include a top sheet and bottom sheet of planar doping of highly doped p-material separated by a lightly doped layer of p-material, whereby said top sheet achieves low gate contact resistance and said bottom sheet defines the capacitance of said n-channel FET transistor.

51. A method of fabricating an optoelectronic integrated circuit according to claim 44, further comprising:

coupling a current source to said injector terminal such that said current source draws bias current from a quantum well structure coupled thereto, and

coupling a load resistor to said cathode terminal such that a forward bias exists between said anode and cathode terminals that is less than maximum forward switching voltage of the thyristor device.

52. A method of fabricating an optoelectronic integrated circuit according to claim 51, wherein:

said given thyristor device is configured as an optical detector that detects an incident optical pulse of sufficient intensity at an associated wavelength and produces a corresponding output electrical pulse at the cathode terminal of said given thyristor device.

53. A method of fabricating an optoelectronic integrated circuit according to claim 52, wherein:

said given thyristor device is configured such that when said incident optical pulse has sufficient intensity at the associated wavelength, photocurrent is produced in said quantum well channel in excess of said bias current to produce a channel charge that exceeds a critical switching charge, thereby causing said thyristor device to switch to the ON state, and when the incident optical pulse is terminated, the bias current switches the thyristor device to the OFF state.

54. A method of fabricating an optoelectronic integrated circuit according to claim 53, wherein:

said given thyristor device is configured as a laser emitter that emits an output optical pulse at an associated wavelength in response to an input electrical pulse supplied to the injector terminal.

55. A method of fabricating an optoelectronic integrated circuit according to claim 54, wherein:

said given thyristor device is configured such that said input electrical pulse produces current in said quantum well channel in excess of said bias current to produce a channel charge that exceeds a critical switching charge, thereby causing said thyristor device to switch to the ON state, and when the input electrical pulse is terminated, the bias current switches the thyristor device to the OFF state, and wherein current through the given thyristor device in the ON state is greater than a characteristic lasing threshold current for the given thyristor device.

56. A method of fabricating an optoelectronic integrated circuit according to claim 30, wherein:

said resonant cavities comprise a bottom distributed bragg reflector mirror and a top dielectric mirror.

57. A method of fabricating an optoelectronic integrated circuit according to claim 56, wherein:

said thyristor devices are formed from an active device structured disposed between said bottom distributed bragg reflector mirror and said top dielectric mirror, and said portions of said multilayer structure that are removed to provide said resonant cavities with different vertical dimensions are disposed between said active device structure and said top dielectric mirror.

58. A method of fabricating an optoelectronic integrated circuit according to claim 56, wherein:

said resonant cavities include a plurality of diffraction gratings formed under said top dielectric mirror, wherein said diffraction gratings inject incident light that is propagating along an in-plane direction into the resonant cavities and/or emit light produced in the resonant cavities along an in-plane direction.

59. A method of fabricating an optoelectronic circuit according to claim 30, wherein:

N patterning and etching operations performed on said multilayer structure provide said resonant cavities with 2^N different vertical dimensions that correspond to 2^N different wavelengths.